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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,815	12/22/2000	Jean-Didier Allegrucci	3242P008	8894

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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	**PAPER NUMBER**
2187	18

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,815	ALLEGRUCCI ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed May 28, 2004, in response to PTO Office Action dated February 20, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-15 have been presented for examination in this application. In response to the last Office Action, claims 1, 4, 6, 9, 11, and 14 have been amended.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 6, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci et al. (US# 6,518,787) and Wildgrube et al. (US# 6,487,655).

Regarding claim 1, Allegrucci et al. teaches **a configurable system-on-chip, with at least a central processing unit, an internal bus, programmable**

input/output, and programmable logic on a single integrated circuit device (col. 1, lines 14-27).

The difference between the claimed subject matter and that of Allegrucci et al. is that the claim recites executing code from a ROM with a memory alias, searching for a secondary initialization routine to configure the system including system peripherals, locating a configuration program in the ROM, disabling the internal memory alias, and jumping to the secondary initialization routine located in a Flash memory. Wildgrube et al. teaches a computer system with primary and secondary initialization instructions, including **a method for executing code from a ROM** (flash ROM [116b]; col. 3, lines 8-14; col. 4, lines 40-45) **with a memory alias** (predetermined address range), **searching for a secondary initialization routine to configure the system including system peripherals** (col. 6, lines 22-28; col. 5, lines 2-7; 'peripherals' corresponding to PCI and USB devices), **locating a configuration program in the ROM** (col. 5, lines 58-65), **disabling the internal memory alias, and jumping to the secondary initialization routine located in a Flash memory** (col. 6, lines 20-22; 'disabling' and 'jumping' corresponding to transferal of execution control).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Allegrucci et al. and Wildgrube et al. before him at the time the invention was made to modify the CSOC to include the primary and secondary initialization instructions, because then the cooperative primary and secondary initialization would replace the unfriendly and error prone BIOS updating, as taught by Wildgrube et al. (col. 1, lines 44-49).

Regarding claim 5, Allegrucci et al. teaches where **the alias of the internal ROM memory is programmed** such that the primary initialization instructions are first given control (**priority over the secondary initialization instructions [external alias]**) (col. 5, lines 58-65). The **external alias of the FLASH memory** is inherently **programmed** and known to the system of Allegrucci et al. such that secondary initialization instructions are located and processed when initialization control automatically switches from the primary initialization instructions to the secondary initialization instructions. (col. 6, lines 19-27).

Regarding claim 6, Allegrucci et al. teaches **a configurable system-on-chip, with at least a central processing unit, an internal bus, programmable input/output, and programmable logic on a single integrated circuit device** (col. 1, lines 14-27). The difference between the claimed subject matter and that of Allegrucci et al. is that the claim recites executing code from an internal memory with a memory alias, searching for a secondary initialization routine to configure the system including system peripherals, locating a configuration program in the internal memory, disabling the internal memory alias, and jumping to the secondary initialization routine. Wildgrube et al. teaches a computer system with primary and secondary initialization instructions, including **an apparatus for executing code from an internal memory** (flash ROM [116b]; col. 3, lines 8-14; col. 4, lines 40-45) **with a memory alias** (predetermined address range), **searching for a secondary initialization routine to configure**

the system including system peripherals (col. 6, lines 22-28; col. 5, lines 2-7; 'peripherals' corresponding to PCI and USB devices), **locating a configuration program in the internal memory** (col. 5, lines 58-65), **disabling the internal memory alias, and jumping to the secondary initialization routine** (col. 6, lines 20-22; 'disabling' and 'jumping' corresponding to transferal of execution control).

Regarding claim 11, Allegrucci et al. teaches **a configurable system-on-chip, with at least a central processing unit, an internal bus, programmable input/output, and programmable logic on a single integrated circuit device** (col. 1, lines 14-27). The difference between the claimed subject matter and that of Allegrucci et al. is that the claim recites executing code from an internal memory with a memory alias, searching for a secondary initialization routine to configure the system including system peripherals, locating a configuration program in the internal memory, disabling the internal memory alias, and jumping to the secondary initialization routine. Wildgrube et al. teaches a computer system with primary and secondary initialization instructions, including **a computer readable medium** (Flash ROMs) **with instructions for executing code from an internal memory** (flash ROM [116b]; col. 3, lines 8-14; col. 4, lines 40-45) **with a memory alias** (predetermined address range), **searching for a secondary initialization routine to configure the system including system peripherals** (col. 6, lines 22-28; col. 5, lines 2-7; 'peripherals' corresponding to PCI and USB devices), **locating a configuration program in the internal**

memory (col. 5, lines 58-65), **disabling the internal memory alias, and jumping to the secondary initialization routine** (col. 6, lines 20-22; 'disabling' and 'jumping' corresponding to transferal of execution control).

Claims 2, 3, 7, 8, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci et al. (US# 6,518,787) and Wildgrube et al. (US# 6,487,655) as applied to claims 1, 5, 6, and 11 above, and further in view of Bealkowski et al. (US# 5,327,531).

Allegrucci et al. and Wildgrube et al. teach a CSOC as described above in regards to claims 1, 5, 6, and 11. The difference between the claimed subject matter of claims 7 and 12 and that of Allegrucci et al. and Wildgrube et al. is that the claims recite configuring the CSOC using the secondary initialization routine. Bealkowski et al. teaches **configuring the CSOC using the secondary initialization routine** (col. 2, lines 49-68). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Allegrucci et al., Wildgrube et al., and Bealkowski et al. before him at the time the invention was made to modify the CSOC to include the CSOC secondary initialization instructions, because then the secondary resource could be used as an alternative should the primary resource holding the primary initialization commands become corrupted (col. 2, lines 61-64).

Regarding claim 2, Allegrucci et al. and Wildgrube et al. teach a CSOC as described above in regards to claims 1, 6, and 11. Wildgrube et al. also teaches using a secondary **flash (external) memory** for storing secondary initialization routines. The difference between the claimed subject matter and that of Allegrucci et al. and Wildgrube et al. is that the claims recite configuring the CSOC using the secondary initialization routine. Bealkowski et al. teaches **configuring the CSOC using the secondary initialization routine** (col. 2, lines 49-68).

Regarding claims 3, 8, and 13, Wildgrube et al. teaches **resetting a CPU of the CSOC** (abs., lines 13-17).

Claims 4, 9, 10, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci et al. (US# 6,518,787), Wildgrube et al. (US# 6,487,655), and Bealkowski et al. (US# 5,327,531) as applied to claims 2, 3, 7, 8, 12, and 13 above, and further in view of Bartoli et al. (US# (US# 6,401,164).

The difference between the claimed subject matter and that of Allegrucci et al., Wildgrube et al., and Bealkowski et al., disclosed supra, is that claims 4, 9, and 14 recite that code is executed in a manner starting from the bottom of the external memory, and specifically from the bottom of a FLASH memory in claim 4. Bartoli et al. teaches both top and **bottom boot sector** configurations for a **memory device** (Figures 1A & 1B; col. 1, line 49 – col. 2, line 19), which is also a **FLASH memory** as applied to claim 4. Therefore it would have been obvious

to one of ordinary skill in the art having the teachings of Allegrucci et al., Wildgrube et al., Bealkowski et al., and Bartoli et al. before him at the time the invention was made to modify the external memory of Allegrucci et al., Wildgrube et al., and Bealkowski et al., to include code executing from the bottom of a FLASH memory, because then a (FLASH) memory with both top and bottom selectable boot sectors could be incorporated in order to facilitate market demands (col. 1, lines 41-43). Also, reduced manufacturing costs would be incurred by incorporating the Bartoli et al. invention such that a single memory with a selectable top and bottom boot sector could be used when a preference for an upper or lower boot sector is specifically preferred (col. 2, lines 58-63).

Regarding claims 10 and 15, Wildgrube et al. teaches **setting up an application program** (system initialization) **for the system-on-chip** (of Allegrucci et al.) **from the internal memory** (flash ROM [116b]; col. 3, lines 8-14; col. 4, lines 40-45).

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to other secondary initialization schemes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

July 8, 2004

Brian R. Peugh
Patent Examiner
Art Unit 2187